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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,165	04/27/2001	Shinichi Kobayashi	57454-093	2071

7590 10/21/2008

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EXAMINER
LE, VU ANH

ART UNIT	PAPER NUMBER
2824	

MAIL DATE	DELIVERY MODE
10/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/843,165	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-8* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/841,372.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 5-6 are rejected under 35 U.S.C. 102(a) as being anticipated by Montalvo et al (5,126,808).

3. With respect to claim 1, Montalvo et al (Fig.5) discloses a nonvolatile semiconductor memory device comprising: a semiconductor substrate; a main bit line formed of metal wiring on said substrate (array bit line BL0 to BLk made of second metal level, col.9, line 63); first and second sub bit lines connected in series, each formed of metal wiring and aligned parallel to said main bit line on said substrate (the first and second sub bit lines are in series and made of first level metal, BLK-0, BLK-1... in Fig.5 and col.9, lines 59-66); first and second switching transistors ((0,k) to (m,k) transistors in Fig.5), each responsive to a sector select signal (PgSEL0) for connecting said main bit line to a corresponding one of said first and second subbit lines, a first memory cell group including a plurality of memory cells ((00,k) to (0n,-k) memory cells), each connected to said first sub bit line; and a second memory cell group including a plurality of memory cells ((10,k) to (1n,-k) memory cells), each connected to said second sub bit line; wherein at least a part of the main bit line and at least a part of the

sub bit lines are formed in different layers (the main bit lien and the first and second sub bit lines are on two different metal layers, the first level metal layer and the second level metal layer), each of said memory cells includes a control gate and a floating gate formed on said substrate (Fig.5), and a source and a drain formed in a substrate area, and each of said memory cells is connected to a corresponding one of said first and second sub bit lines via said drain (inherent); said device further comprising an insulating layer formed in a substrate area for insulating a memory cell in said first memory cell group located closest to said second memory cell group from a memory cell in said second memory cell group located closest to said first memory cell group (inherent).

With respect to claims 5-6. Montalvo et al (Fig.5) disclose a nonvolatile semiconductor memory device, comprising: a first bit line (array bit line BLk, see col.9, line 63) formed of metal wiring; a switch (switch (0,k), Fig.5) having an end connected to said first bit line (BLk); a second bit line (page bit line BLk-0, see col.9, lines 59 and 61) formed of metal wiring and connected to other end of said switch; and a plurality of memory cells connected to said second bit line (Fig.5), each including a drain, a control gate, a floating gate and a source, wherein at least a part of the first bit line and at least a part of the second bit line are formed in different layers (col.9, lines 64-65 teach “Each second level metal bit line is located directly over but insulated from the corresponding first metal page bit line), wherein said first bit line is placed in an upper layer of said second bit line.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yiu et al (5,526,307) in view of Montalvo et al (5,126,808).

Yiu et al (Figures 1 and 2) disclose a nonvolatile semiconductor memory device (100, Fig.1 and Fig.2) having all the features as claimed, such as a main bit line (84) ***formed of metal wiring on said substrate (see col.3, line 3 or col.7, line 24)***, first and second subbit lines (80 upper part and lower part) connected in series, each aligned parallel to said main bit line; first and second switching transistors (82 upper part and lower part), each for connecting said main bit line to a corresponding one of said first and second subbit lines (see Fig.2); a first memory cell group (76-N) including n (n_>2) memory cells, each connected to said first subbit line; a second memory cell group (76-N) including n (n_>2) memory cells, each connected to said second subbit line (the other group of memory cells in the lower part), wherein each of said memory cells includes a control gate, a floating gate, a drain and a source, and each of said memory cells is connected to a corresponding one of said first and second subbit lines via

said.drain, said device further comprising: n connection lines (WL1), each for connecting the control gate of a relevant memory cell (76-N upper part) in said first memory cell group to the control gate of a corresponding memory cell (76-N lower part) in said second memory cell group; and a row decoder (104, Fig.1), responsive to an externally applied address signal for selecting one of said n connection lines.

Yiu et al fails to disclose first and second subbit line formed of metal wiring and a main bit line and subbit line are formed in different layers.

Montalvo et al disclose a memory device having first and second subbit line formed of metal wiring and a main bit line and subbit line are formed in different layers (see col.9, lines 59-66 and Fig.5).

Thus, it would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Yiu et al by metal subbit line and make a main bit line and subbit line in different layers such as taught by Montalvo et al in order to increase the speed of memory operation.

6. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montalvo et al in view of Gotou (5,051,952).

7. With respect to claim 8, Montalvo et al disclose all the features as claimed except for the second bit line formed of polycrystalline silicon. Gotou disclose a memory device having main bit lines made of metal (Al) and sub bit lines made of polysilicon (col.7, line 51-53). Thus, it would have been obvious to one of ordinary skill in the art at the time

this invention was made to modify Montalvo et al by using sub bit line made of polysilicon as second bit line such as taught by Gotou in order to simplify the process of fabricating a memory device.

8. With respect to claim 7, Gotou also discloses a source line formed with an active layer, to which said sources of said memory cells are commonly connected (col.8, lines 23-27).

Allowable Subject Matter

9. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: claim 4 recites an allowable feature of " n connection lines are formed of polycrystalline silicon, and wiring for connection between said row decoder and said n connecting lines is formed of metal wiring".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vu A. Le/

Primary Examiner, Art Unit 2824

Vu A. Le
Primary Examiner
Art Unit 2824

10/19/2008